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REMARKS

In reply to the Final Office Action of May 7, 2004, Applicant submits the following remarks.

Applicant thanks the Examiner for allowing claims 39 and 40, and for the indication of allowable subject matter in claim 9. Applicant also thanks the Examiner for the interview conducted at the Patent and Trademark Office on June 24, 2004. The Examiner prepared an Interview Summary and this Remarks section also includes a summary of various points addressed in the interview.

In particular, the Examiner agreed that Rozenblit did not appear to disclose at least a "switch operable to switch . . . between the first output signal and the second output signal . . . based on at least one of a first lock indicator signal and a second lock indicator signal," as recited in claim 1. This position is explained below in the "Lack of Disclosure" section under the discussion of claims 1 and 21. The Examiner also agreed to review the motivation to combine the references, and Applicant's position that there is no motivation is explained below in the "Lack of Motivation to Combine" section under the discussion of claims 1 and 21.

Claims 1-21, 23, 28, 29, and 32-42 were examined. No claims have been amended or added. Claims 32, 33, and 41 have been cancelled. Claims 1, 14, 21, 38, 39, and 40 are independent.

Independent Claims 1 and 21

Claims 1-5, 8, 13, 21, 29, 34-36, and 42, each of which depends from claims 1 or 21, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson (4,463,612) in view of Rozenblit (6,466,069) and further in view of Ims (3,751,979) and Olgaard (6,236,278). Applicant respectfully disagrees because, at least, there is no motivation for the combination, and the combination does not disclose or suggest each of the recitations of independent claims 1 or 21.

- Lack of Motivation to Combine

Regarding the lack of motivation, Applicant submits that there is no motivation to modify Thompson with Rozenblit, or to modify the combination of Thompson and Rozenblit with Ims.

First, Applicant submits that the there is no motivation to modify Thompson with Rozenblit. The Office Action appears to have interpreted Applicant's earlier remarks as being directed to a modification of Rozenblit by Thompson. Applicant submits that the earlier remarks are applicable to a modification of Thompson by Rozenblit, and provides the following remarks in to clarify why there is no motivation to modify Thompson with Rozenblit.

The application described by Rozenblit is that of a PLL being used to generate a VCO clock at a selectable frequency based off of a REF CLK. The PLL is not tracking a variable signal, as in a vortex flow meter, but a fixed REF CLK. Rozenblit describes the use of a divider 170 to allow the VCO frequency to be modified.

Because the REF CLK can introduce noise onto the VCO output signal (col. 7, lines 56-59), Rozenblit describes a system in which a PLL is operated in either a slow mode having a small bandwidth which passes less noise, or a fast mode having a large bandwidth passing more noise but also changing frequency faster than the slow mode (col. 5, lines 58-67 and lines 29-40; col. 7, lines 56-65). Rozenblit teaches the use of a "change bandwidth signal 130" to indicate whether the slow mode (for low noise) or the fast mode (for quick response) is desired, and to cause the PLL to move into the desired mode. Rozenblit does not teach how the "change bandwidth signal" is generated, but indicates that the "change bandwidth signal" is changed before the frequency changes. See, for example, (i) col. 5, lines 59-61, stating that the "change bandwidth signal switches . . . indicating a change in the bandwidth . . . is desired" (emphasis added), and (ii) col. 8, lines 21-25 (and Fig. 3), stating that "a change in the desired frequency . . . is detected. For example, a control signal may be received that indicates a change in the desired frequency" (emphasis added). By switching the "change bandwidth signal" before changing frequency, the PLL of Rozenblit is allowed to move out of the slow mode (see col. 5, lines 29-32) before the frequency begins to change, so that the PLL can track the frequency in the fast mode when the frequency does change (see col. 7, lines 63-65).

Thompson describes a single PLL and does not describe or suggest changing the characteristics of the PLL. The PLL of Thompson is used to track a vortex frequency signal that changes unexpectedly (see, e.g., col. 1, lines 23-28; col. 3, lines 14-15 and 24-30). As a result, Thompson does not know when a frequency change will occur, as does Rozenblit, and can also lose lock from an unexpected frequency change.

If Thompson were modified to include the PLL of Rozenblit, Thompson would be unable to provide a signal to the PLL to indicate that a frequency change was desired because Thompson does not know when a frequency change is going to occur in the vortex signal being received. Further, the PLL in the proposed modification of Thompson by Rozenblit would be in slow mode when the vortex signal was relatively static, as taught by Rozenblit, and would presumably lose lock when an unexpected and large change in the vortex frequency was encountered. For at least these reasons, there is no motivation to modify Thompson to include the PLL of Rozenblit because the proposed combination would not work.

Second, Applicant submits that the there is no motivation to modify a Thompson/Rozenblit combination with Ims. The teaching in Ims to use two PLLs arises in the particular context of two different input signals, in which a single PLL cannot remain locked to both input signals. A Thompson/Rozenblit combination presents the opposite context of having a single input signal to which a single PLL can remain locked, and there is no motivation to use two PLLs or to consider the teaching of Ims.

Ims describes a system in Figure 8 having two separate input signals that are separately fed into two fixed-bandwidth PLLs. The output from each of the two PLLs goes to switch 208, and the output of switch 208 serves as the input to a computation unit 70. Computation unit 70 determines which input signal is to be processed and controls switch 208 using a control signal to tell switch 208 which PLL to select.

Because Ims has two PLLs that each operate on a different input signal, Ims provides no motivation to modify a Thompson/Rozenblit combination to have two PLLs operating on the same input signal. Ims does not suggest that such a modification would be possible, much less beneficial, and so a person of ordinary skill in the art would not draw from Ims the motivation to make such a modification.

Ims may teach that a system with two PLLs operating in parallel on separate input signals is faster than a system with a single PLL switching between the two separate input signals. Such a teaching, however, is not germane to the Thompson/Rozenblit combination or the claimed invention, which have only a single input signal. The motivation in Ims for using two PLLs arises precisely because Ims has two separate input signals, and one PLL cannot be locked to

both signals at the same time. However, in the Thompson/Rozenblit combination and the claimed invention, there is only one input signal and a single PLL can remain locked to the single input signal. Accordingly, even the motivation in Ims to use two PLLs would not motivate a person of ordinary skill in the art to use two PLLs in a Thompson/Rozenblit combination.

The Office Action appears to argue in the alternative that the motivation to combine Ims may be found in the general knowledge available to one of ordinary skill (pages 18-19 of the Office Action). The Office Action states that "one having ordinary skill in the art would recognize that by providing two PLLs, each operating at a different bandwidth[] and providing a means for switching between the PLLs as needed, rather than providing one PLL that must be modified to operate at the needed bandwidth, would result in a faster, simpler operation" (page 18). The Office Action further asserts that "switching between two operating PLLs would only depend on the switching time, which would be faster than the capacitor [of Rozenblit] charging/discharging" (page 19).

Applicant disagrees with the assertions quoted above in which the Office Action proposes that one PLL should be replaced with two. Switching between two PLLs introduces switching noise and requires two additional components—the switch and the second PLL—which add cost and heat and require space. All of these increased factors (noise, cost, heat, space) are generally avoided in designs. Additionally, Rozenblit teaches explicitly that the charge pump "can switch rapidly" and that "[t]he switching speed can be adjusted by adjusting the rate the capacitor 122 charges up and discharges" (col. 5, lines 37-40). Given that Rozenblit teaches how to increase the charge pump's switching speed, and given the drawbacks of the modification proposed by the Office Action, Applicant asserts that there is no motivation for the proposed modification.

- Lack of Disclosure

Regarding the lack of disclosure, the combination does not disclose or suggest at least:

(i) the claimed "switch operable to switch . . . between the first output signal and the second output signal in response to a change in the frequency [of the input signal], and based on at least one of a first lock indicator signal and a second lock indicator signal" (claim 1),

"switching . . . from an output signal of the first PLL to an output signal of the second PLL when the lock indicator signal indicates that the second PLL is locked" (claim 21), or

"switching . . . from the output signal of the second PLL to the output signal of the first PLL when the lock indicator signal indicates that the second PLL is out of lock" (claim 21), or

(ii) the claimed "a first phase-locked loop . . . operable to lock into a frequency of an input signal" and "a second phase-locked loop . . . operable to lock into the frequency of the input signal" (claim 1),

"locking into a frequency of the input signal using the first PLL" (claim 21), or

"locking into the frequency of the input signal . . . using the second PLL" (claim 21).

First, the combination of references does not disclose or suggest the claimed "switch operable to switch . . . between the first output signal and the second output signal in response to a change in the frequency [of the input signal], and based on at least one of a first lock indicator signal and a second lock indicator signal" (claim 1) or the "switching" recitations of claim 21 quoted above.

Neither Thompson nor Rozenblit have a switch or switch between PLL outputs, as the Office Action acknowledges by looking to Ims for a switch (page 4 of the Office Action).

Rozenblit does describe changing the bandwidth of a single PLL, however, and the Office Action further states that Rozenblit performs the bandwidth change "based upon a determination that the phase locked loop is locked (column 4, lines 28-32)" (page 4 of the Office Action, see also pages 5 and 6). Applicant disagrees. In the passage cited by the Office Action, Rozenblit merely notes that the PLL can be in lock, observing that "[w]hen the two input signals [to the PLL] are in phase, the PLL 100 is locked" (col. 4, lines 30-31).

Further, Rozenblit does not change the bandwidth of the PLL (much less "switch") based on any "lock" information. In particular, Rozenblit does not change bandwidth "based on . . . a . . . lock indicator signal" as recited in claim 1, or when a lock indicator signal has a particular indication (see claim 21), but rather changes the bandwidth based on a "change bandwidth" signal which indicates that a bandwidth change is desired (col. 5, lines 60-61; col. 8, lines 23-25). Rozenblit changes between a fast mode and a slow mode based entirely on the change bandwidth signal, which modifies Vref 146 (col. 5, lines 7-40; see also cols. 1-2). In particular, the change in mode in Rozenblit is not based on the input frequencies, the UP or DW signals, or

whether the PLL is in phase (see col. 5, lines 29-35 describing that the mode is determined by Vref, and lines 23-29 describing that Vref is determined by the "change bandwidth signal").

Additionally, it should be clear that Rozenblit does not change mode "in response to a change in the frequency" as recited in claim 1. Rather, the implementation described by Rozenblit changes mode in anticipation of (not in response to) a desired change in the frequency.

Ims does have a switch 208, but switch 208 does not meet the claimed limitations. As explained above, switch 208 does not switch "in response to a change in frequency" (claim 1), but in response to the control signal; no change in frequency is required. Switch 208 also does not switch "based on . . . a . . . lock indicator signal" (claim 1) or when a lock indicator signal ahs a particular indication (see claim 21), but based on the control signal. Indeed, Ims describes switching to a PLL that is out of lock (Fig. 5; col. 16, lines 45-55), as well as switching to a PLL that is in lock (Fig. 8; col. 16, lines 45-55), revealing that the decision to switch in Ims is not related to whether the PLLs are locked.

The Office Action states that Ims switches PLLs "in response to a change in the frequency (column 6, lines 25-46 and column 16, lines 29-33)" (page 4 of the Office Action). Applicant disagrees. Both cited passages describe using a control signal on line 78 to control a switch (either switch 88 of Fig. 5 or switch 208 of Fig. 8), as described above, and do not describe switching "in response to a change in the frequency."

Olgaard does not make up for the deficiencies of Thompson, Rozenblit, and Ims. For example, Olgaard does not disclose or suggest a system having more than one PLL and, therefore, does not disclose or suggest "switch[ing] . . . between the first output signal [of a first PLL] and the second output signal [of a second PLL]" (claim 1), or "switching . . . from an output signal of the first PLL to an output signal of the second PLL" (claim 21).

Second, the combination of references does not disclose or suggest at least "a first phase-locked loop . . . operable to lock into a frequency of an input signal" and "a second phase-locked loop . . . operable to lock into the frequency of the input signal" (claim 1), or "locking into a frequency of the input signal using the first PLL" and "the second PLL" (claim 21).

Thompson and Rozenblit each have only one PLL, as the Office Action acknowledges (page 4 of the Office Action).

Ims has two PLLs, but the two PLLs are not both "operable to lock into the frequency of the input signal." That is, Ims's PLLs do not both lock onto the same input signal, much less the same frequency of the same input signal. As described above, Ims has two separate input signals, and each input signal has its own PLL (Fig. 8 of Ims).

Olgaard does not make up for the deficiencies of Thompson, Rozenblit, and Ims. For example, Olgaard does not disclose or suggest a system having more than one PLL and, therefore, does not disclose or suggest "a first phase-locked loop" and "a second phase-locked loop" (claim 1), or ""locking into a frequency of the input signal using the first PLL" and "the second PLL" (claim 21).

Accordingly, for at least these reasons Applicant submits that a *prima facie* case of obviousness has not been established with respect to claims 1 and 21 and claims that depend therefrom and, in the alternative, that such claims are patentable over the applied references.

Independent Claim 14

Claims 14-19 and 37, each of which depends from claim 14, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit, Ims, and Olgaard, and further in view of Vignos (5,576,497). Applicant respectfully disagrees for at least the reasons that, as explained in the above discussion of claim 1, (i) there is no motivation for the combination, and (ii) the combination does not disclose or suggest claim 14's recitation of "a switch for switching . . . among the PLL output signals in response to a change in the frequency, and based on one or more lock indicator signals" (claim14). Accordingly, for at least these reasons Applicant submits that a *prima facie* case of obviousness has not been established with respect to claim 14 and claims that depend therefrom and, in the alternative, that such claims are patentable over the applied references.

Claims 6 and 7, each of which depends from claim 1, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit, Ims, and Olgaard, and further in view of Bouillet (6,298,100). Applicant respectfully disagrees for at least the reasons discussed above with respect to claim 1.

Claims 10-12, each of which depends from claim 1, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit, Ims, and Olgaard, and further

in view of Henry (5,570,300). Applicant respectfully disagrees for at least the reasons discussed above with respect to claim 1.

Independent Claim 38

Claim 20 (which depends from claim 1) and claim 38 both stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit, Ims, Olgaard, and Vignos and further in view of Ito (4,201,084). Applicant respectfully disagrees. With respect to claim 20, Applicant submits that the rejection is overcome for at least the reasons discussed above with respect to claim 1. With respect to claim 38, Applicant submits that the rejection is overcome for at least the reasons that, as explained in the above discussion of claim 1, (i) there is no motivation for the combination, and (ii) the combination does not disclose or suggest claim 38's multiple-PLL recitation of "phase-locked loops (PLLs) having different characteristics from each other and operable to receive the flow sensor signal and lock onto the flow sensor signal" (claim 38). Accordingly, for at least these reasons Applicant submits that a *prima facie* case of obviousness has not been established with respect to claim 38 and claims that depend therefrom and, in the alternative, that such claims are patentable over the applied references.

Claims 32, 33, and 41, each of which depends from claim 32, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Vignos and further in view of Henry. This rejection is moot in light of Applicant cancelling claims 32, 33, and 41.

Claim 23 (which depends from claim 1) and claim 28 (which depends from claim 21) both stand rejected as being unpatentable over Thompson in view of Rozenblit, Ims, and Olgaard and further in view of Yatsuzuka (5,128,625). Applicant respectfully disagrees for at least the reasons discussed above with respect to claims 1 and 21.

The Office Action stated that references AM and BG were not considered from the Information Disclosure Statement filed on February 24, 2004. With respect to reference AM (selected portions of Chapter 9 of Phase-Lock Basics), the Office Action indicated that no copy of reference AM was received. In response, Applicant has attached another copy of reference AM, along with a copy of the stamped postcard showing that the PTO received 25 references on February 24, 2004. As there were only 25 references on the Form PTO-1449, the PTO is presumed to have received a copy of each of the 25 references. Accordingly, the IDS filed on February 24, 2004, should be considered to have been complete and the provision of the

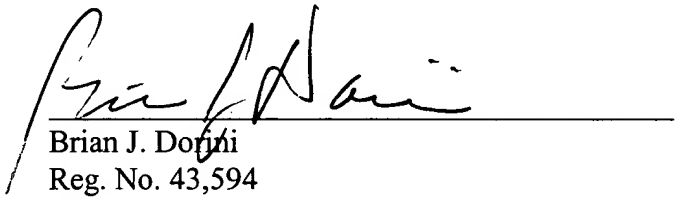
additional copy herewith is not a supplemental IDS. With respect to reference BG (a British standard), the Office Action indicated that reference BG appeared to be substantially duplicated by reference AN (an American standard). It is Applicant's understanding that different references, even if cumulative, are each to be considered and initialed. Accordingly, given that the references are different, one relating to a British standard and the other relating to an American standard, Applicant respectfully requests that the Examiner consider and initial both references.

Applicant does not agree with certain of the Office Action's characterizations of the cited references but, for clarity and brevity in argument, have generally not addressed such characterizations unless required by the line of reasoning in the above arguments. Accordingly, Applicant's silence should not be construed as acquiescing in any of the Office Action's characterizations of the cited references.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: JULY 7, 2004



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To Henry P. Nettesheim
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and the zero at 20 kHz. What is K under the following conditions:

(a) The VCO center frequency f_c equals the input frequency f_{in}?

(b) The VCO center frequency f_c is 50 kHz higher than the input frequency f_{in}?

8.4 A loop must have 100-kHz bandwidth. It has a lag-lead filter with a 10-kHz zero frequency. Pull-in range is to be ± 500 kHz.

(a) What is the largest uncompensated phase detector offset that can be tolerated?

(b) What should the filter pole frequency be?

CHAPTER 9

ACQUISITION AIDS

Sometimes the pull-in range is inadequate or acquisition is too slow. An obvious solution is to increase the loop bandwidth, but other considerations, such as a filtering action that may be desired from the loop, can make that impractical. An acquisition aid often provides the solution. It can permit the loop to lock when its mistuning falls between the hold-in range and the pull-in range ($\Omega_{pf} \leq |\Omega| < \Omega_H$) or it can speed up a pull-in that might otherwise be delayed while many cycles are skipped. We will consider several acquisition aids in this chapter.

9.1 COHERENT DETECTION—LOCK INDICATOR

We can use the coherent detector as part of an acquisition aid or to warn when the loop has become unlocked. Detection refers to extraction of a signal proportional to the amplitude (or power[1]) of the detected signal. Coherent detection is a method of detection that employs a second, reference, signal of identical frequency and proper phase. Coherent detection has an advantage of sensitivity over other methods, but the necessity to obtain the reference signal adds complexity.

The coherent detector can be a balanced mixer, structurally identical to the phase detector (in which case $K'_{pd} = K'_p$. The pertinent term in Eq. (3.5) is $\cos[\varphi_1(t) - \varphi_2(t)]$, the same term that produces phase detection. However, for coherent detection, $\varphi_1(t) - \varphi_2(t)$ is approximately 0°, corresponding to

[1] This is called square-law detection.

provide this changing current as the voltage across R_p changes. However, at the moment when there is no voltage across R_p, the phase error will be the same as if R_p were absent. If we call this moment $t = 0$, then we can write Eq. (9.3) as

$$\varphi_e = \{\dot{\omega}_{in} - \dot{\omega}_r\}\left\{\frac{1}{\omega_n^2} + 2\zeta\frac{1-\alpha}{\omega_n}t\right\} = \{\dot{\omega}_{in} - \dot{\omega}_r\}\left\{\frac{1}{\omega_n^2} + \frac{t}{K}\right\}. \quad (9.4)$$

Here t equals t' plus a constant, and the constant is chosen such that, at $t = 0$, when the voltage across R_p is zero, the equation is the same as it would be for an integrator-and-lead filter.

, during steady-state lock (no sweep), $\Delta\varphi = -\pi/2$, then, during sweep, it will be $\Delta\varphi = \varphi_e - \pi/2$, so Eq. (9.1) will become $v_{CD} = K'_{pd}\cos(\varphi_e)$. This is approximately equal to K'_{pd} for small φ_e. For larger errors Eq. (9.4) must be replaced by a form that accounts for the sinusoidal characteristic of the phase detector,[5]

$$\sin(\varphi_e) = \{\dot{\omega}_{in} - \dot{\omega}_r\}\left\{\frac{1}{\omega_n^2} + \frac{t}{K'}\right\}, \quad (9.5)$$

and Eq. (9.1) then becomes

$$v_{CD} = K'_{pd}\cos\varphi_e = K'_{pd}\sqrt{1-\sin^2\varphi_e} = K'_{pd}\sqrt{1-\left\{\{\dot{\omega}_{in} - \dot{\omega}_r\}\left[\frac{1}{\omega_n^2} + \frac{t}{K'}\right]\right\}^2}. \quad (9.6)$$

Thus the output of the coherent detector decreases when ω_{in} or ω_r is swept while the loop maintains phase lock. This must be taken into account in setting the threshold voltage.

9.2 CHANGING LOOP PARAMETERS TEMPORARILY

9.2.1 Coherent Automatic Gain Control

Loop parameters can be changed to speed up acquisition. One method is to control the gain of an amplifier that precedes the circuit in Fig. 9.1 by the output voltage from the coherent detector. This arrangement is shown in Fig. 9.2. It must be done in such a manner that, when the loop is not locked, the gain is maximum. Assuming that the phase detector acts like a multiplier (or a balanced mixer in which the input signal is weak compared to the VCO

[5]This assumes that zero input to the filter occurs when $\Delta\varphi = -90°$.

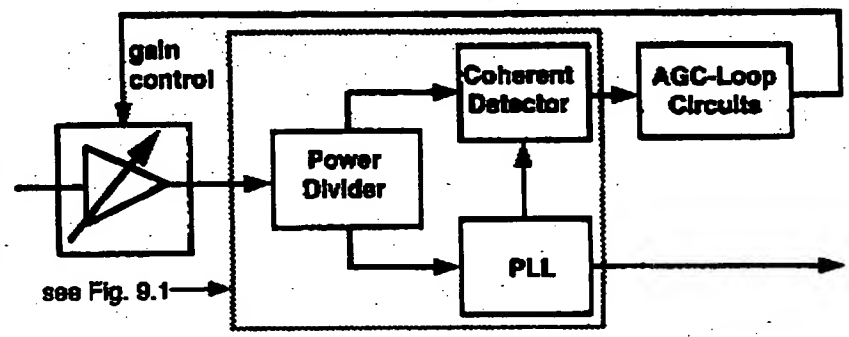

Fig. 9.2 Loop gain control by coherent AGC.

output), the loop gain will then be high because K'_p is proportional to the amplitude of the input signal. When the loop pulls into lock, the output from the coherent detector contains a strong DC component that will pass through the low-pass filter and decrease the preceding amplifier's gain; K'_p will then decrease, resulting in a lower loop bandwidth. This coherently detected voltage can then be used to maintain a constant input level and thus constant phase-locked loop (PLL) parameters. We must ensure that the PLL is stable for all the possible gains as the acquisition process is taking place. Note that the total system now consists of two interdependent loops, the PLL and the automatic gain control (AGC) loop, both of which must be designed for proper performance.

If the AGC loop has high DC gain, it will hold the output of the coherent detector approximately constant, and it will no longer be useful for differentiating between true and false locks. However, the signal that controls the variable-gain amplifier will indicate the strength of the signal at the amplifier's input, and it will thus be useful for false lock detection.

Whether or not coherent AGC is employed, proper false lock detection requires that the strength of the input signal be well enough known. Otherwise we cannot differentiate lock to a weak signal from a DC voltage generated by a strong signal when the loop is not locked. To make this so, it may be necessary to precede the circuit of Fig. 9.1 or 9.2 with a separate, noncoherent, AGC to establish a constant signal level. However, once again, excessive noise can defeat the system by causing the gain to be controlled by the noise rather than the signal.

9.2.2 Filter Modification

We can also modify the loop filter time constants while leaving the low-frequency gain unchanged [Rey, 1960]. During acquisition the filter can be effectively eliminated by shorting the series resistor, possibly turning the loop into a first-order loop. In Fig. 9.3*a*, R_{1A} might represent the series resistance

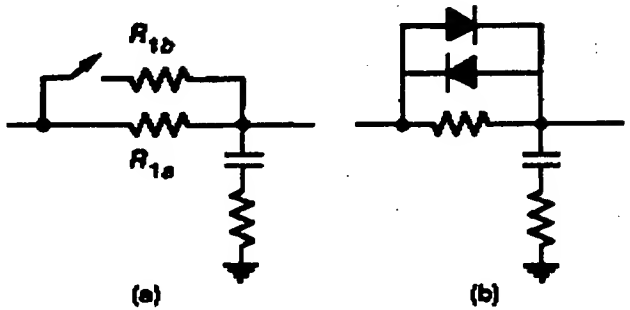

Fig. 9.3 Modification of filter for acquisition.

of the switch, which will usually be a semiconductor device; it could be negligible or it might be purposely added to control gain in the acquisition mode, perhaps to avoid instability. Once acquisition has occurred rapidly in the wide-bandwidth loop, the switch can be opened[6] to restore the desired loop parameters. This process must be controlled from external circuitry, perhaps a timer that is initiated when the loop center frequency is tuned to a new value or the output from a lock indicator such as the coherent detector.

Figure 9.3*b* shows a circuit that automatically widens the bandwidth for large changes in u_1. Once the loop has locked, the changes will be small enough (in the absence of excessive noise) that the diodes will have a very high impedance but, during pull-in, they will conduct and increase the filter pole frequency. The circuit must be carefully planned so this transition occurs at the best point in the pull-in process. There is also a danger that transients from the phase detector (especially from certain digital types) will be large enough to pass through the diodes, thus severely reducing the effectiveness of the filter.

9.2.3 Comparison of Two Types of Parameter Modifications

Figure 9.4 compares the two methods described above by showing the Bode plots of the unmodified loop and of both modified loops.

9.3 AUTOMATIC TUNING OF ω_c, FREQUENCY DISCRIMINATOR

A frequency discriminator can be used to produce a voltage that is proportional to the received frequency and that voltage can be added to u_2 to tune ω_c closer to the input frequency. The quadricorrelator [Richman, 1954b,

[6] We must take care that the switch control signal does not couple excessively into the filter and cause a transient that could undo the progress

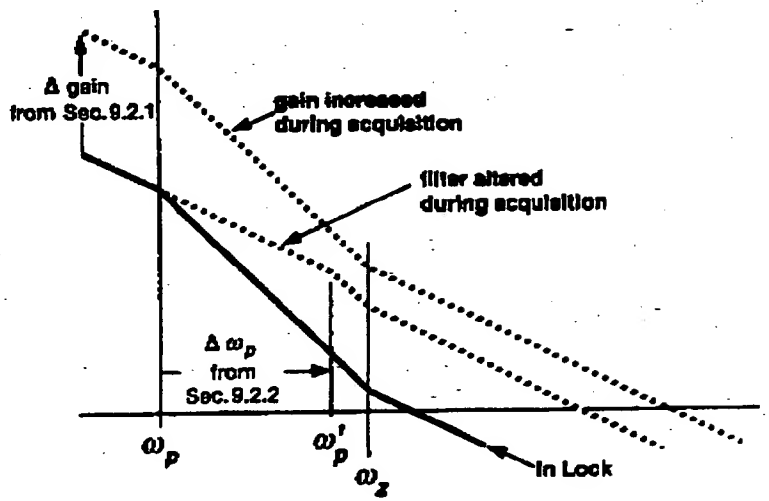

Fig. 9.4 Bode plots corresponding to loop during acquisition. These plots illustrate the modification of loop parameters based on a linearized loop although that is not an accurate representation during much of the pull-in process.

Egan, 1981, p. 243] is a particularly applicable type of discriminator. It produces a voltage that is proportional to the difference between two input frequencies. (The output of an ordinary discriminator is proportional to the frequency offset from some constant value. Thus it is not suitable for indicating the difference between two frequencies that might both be variable. It is also subject to inaccuracies due to component drifts that might change its center frequency or that of the VCO or reference.) This can be used to tune the VCO as shown in Fig. 9.5. At low-frequency errors, its output diminishes so it has little effect on the loop once lock has occurred.

The loop input and the VCO output are compared in two multipliers. One of the signals is shifted by 90° before entering one of the multipliers. As a result, the outputs from the two multipliers, which are at the difference frequency $\Delta\omega$, differ in phase by 90°. One of these is differentiated, giving it a 90° phase shift and a frequency-dependent gain. The two signals that enter the final multiplier are in phase (coherent detection), and one of them has an amplitude that is proportional to $\Delta\omega$. The low-frequency output of the final multiplier is proportional to $-\Delta\omega = \omega_{in} - \omega_{out}$ so it can be added to u_2 in the loop to decrease $\Delta\omega$. Once again, the response of the PLL during pull-in depends on the combined action of two loops. This time a frequency control loop has been added.

Figure 9.6 shows a more practical model of the quadricorrelator. It has amplifiers and the multipliers have been replaced by balanced mixers. The differentiator has been replaced by a high-pass filter, which functions as a

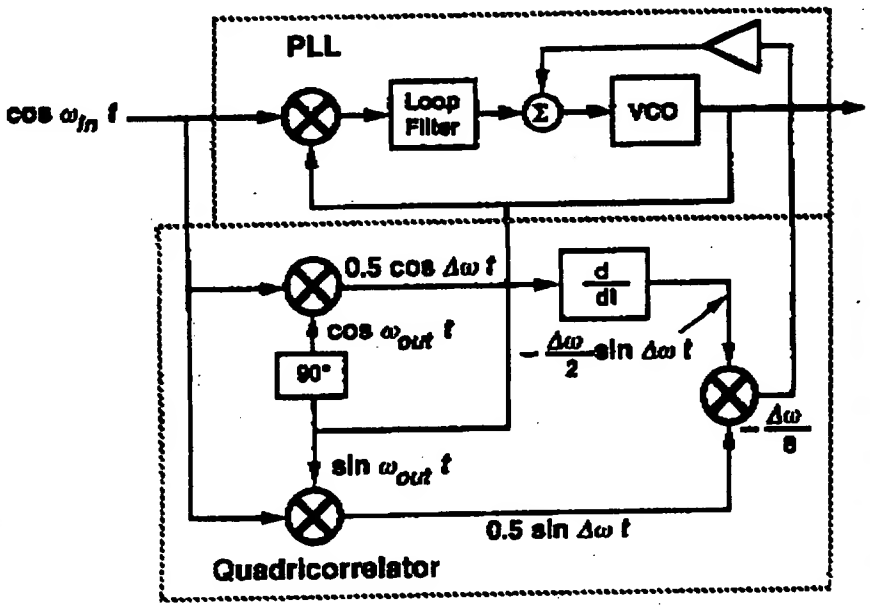

Fig. 9.5 Quadricorrelator concept.

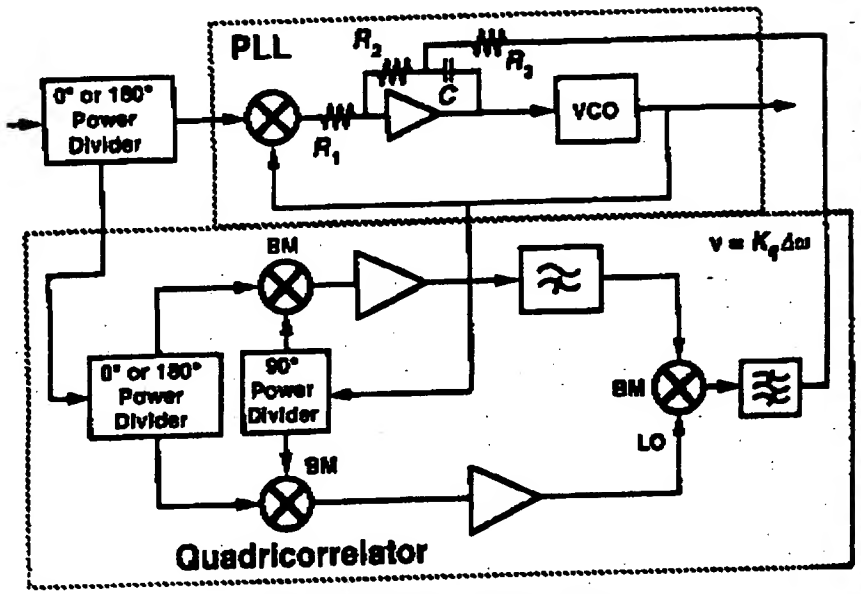

Fig. 9.6 Practical quadricorrelator.

differentiator at frequencies that are well below its cutoff frequency ω_{cu}:

$$F(\omega) = \frac{j\omega}{\omega_{cu} + j\omega} \approx j\frac{\omega}{\omega_{cu}} \qquad \text{for } \omega \ll \omega_{cu}. \tag{9.7}$$

Some options have been shown. A bandpass filter has been placed at the output. We generally assume low-pass function after balanced mixers and multipliers—it eliminates the sum frequency component—but the high-pass function can be added to decrease further the influence of the quadricorrelator on the loop during normal in-lock operation, if desired.

The quadricorrelator output is now shown as being added to the PLL at its loop filter [Gardner, 1979, p. 85]. The loop filter here becomes a filter, an integrator, for the quadricorrelator loop. To see this, assume no DC output from the phase detector (PD), either because the PLL is out of lock or by superposition. Then no current flows through R_1. Since the input to the op-amp is a virtual ground into which no current can flow, no current will then flow through R_2 either, so the junction of C and R_3 is effectively connected to the op-amp input. Since the quadricorrelator otherwise has no pole at the origin (there is no integration to convert frequency to phase as in the PLL), the integrator causes it to change from a zero-order to a first-order loop (to the degree that this integrator is a true integrator).

9.4 ACQUISITION AIDING LOGIC

Several schemes are available that cause the phase detector to aid the acquisition process by becoming effectively a frequency discriminator under conditions where it would otherwise skip cycles (the loop being out of lock) [Egan, 1981, pp. 247–252]. The best known of these is the phase-frequency detector. It is most often used when the signals are, or have been made, digital and is not generally employed in locking to noisy signals.

Compare Fig. 9.7 with Fig. 3.1. The output at C is the same as before, and as before, it goes to 1 (positive) when triggered by the waveform at A. The difference is that, here, B resets the upper flip-flop only indirectly, although the results appear to be the same; B sets the lower flip-flop, which in turn provides a second 1 input to the AND gate (the first being C). This causes a 1 at the AND output, which then resets both flip-flops. The results are the same as before for the case shown. However, if τ should go to zero and then negative, B then preceding A, the results are considerably different. Now the output pulse appears at D and is proportional to $-\tau$. The output at D will eventually be inverted relative to that at C, possibly by entering the opposite input to the loop filter op-amp, so the pulse width at D represents negative phase relative to that at C. This phase detector has a linearly